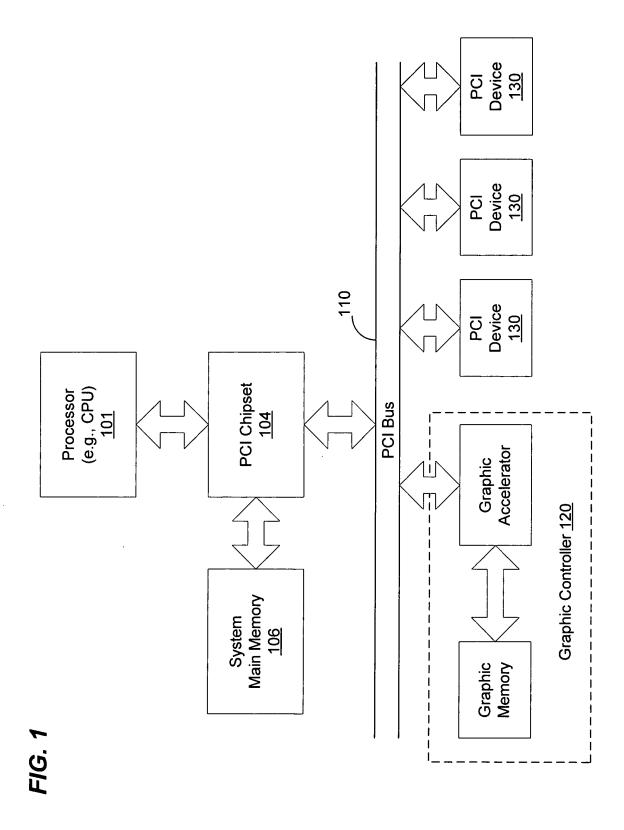
Matter No.: 10559-011003 Page 1 of Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING MECHANISM



Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING
MECHANISM

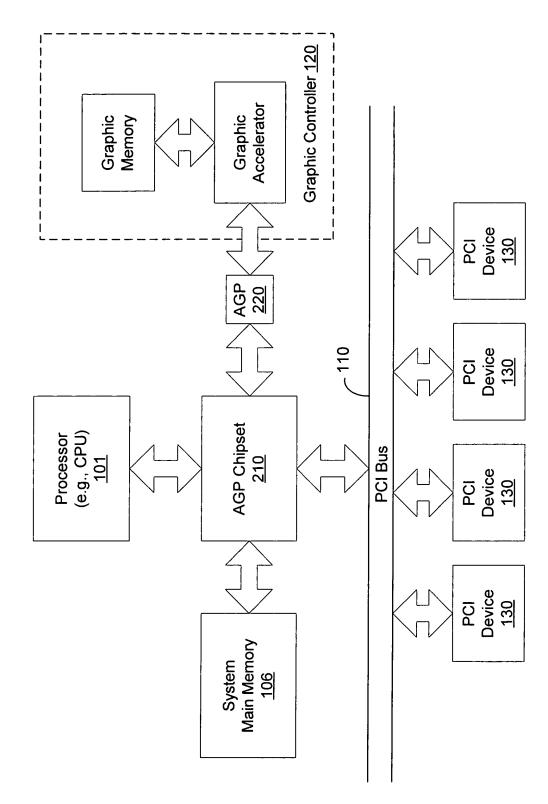
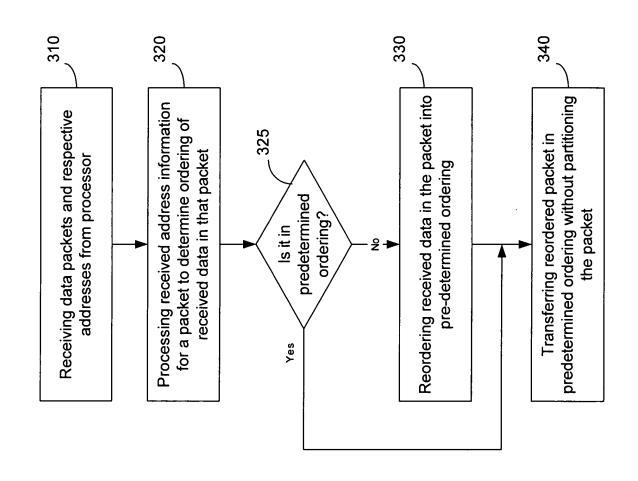


FIG. 2

Page 3 of 12

Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING
MECHANISM

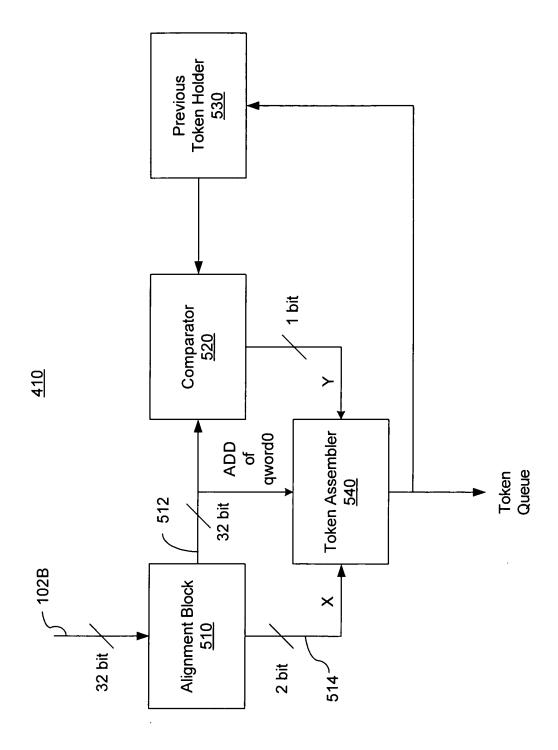


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Page 4 of 12

Page 5 of 12

Matter No.: 10559-011003 Page 5 of Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING MECHANISM



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Matter No.: 10559-011003 Page 6 of Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING MECHANISM

									•		
					TIME				EXE		TIME
								EXE	PRO		
								EXE			
		EXE	CLK7	ARTICLE I				EXE		CLK7	
		EXE	CLK6					EXE		CLK6	
	EXE	PRO	CLK5				EXE	PRO		CLK5	
	EXE		CLK4				EXE			CLK4	
EXE	PRO		CLK3				EXE			CLK3	
EXE			CLK2				EXE			CLK2	
PRO			CLK1				PRO			CLK1	
Token 1	Token 2	Token 3			FIG. 6B		Token 1	Token 2	Token 3		
	PRO EXE	PRO EXE EXE PRO EXE	PRO EXE EXE EXE PRO EXE PRO EXE	PRO EXE EXE PRO EXE EXE PRO EXE CLK1 CLK2 CLK3 CLK4 CLK5 CLK6	PRO EXE EXE PRO EXE EXE CLK1 CLK2 CLK3 CLK4 CLK5 CLK6 CLK7	PRO EXE EXE PRO EXE EXE CLK1 CLK2 CLK3 CLK6	PRO EXE EXE PRO EXE EXE PRO EXE EXE CLK1 CLK2 CLK3 CLK4 CLK5 CLK7	PRO EXE EXE PRO EXE EXE PRO EXE EXE CLK1 CLK3 CLK4 CLK5 CLK7 PRO EXE EXE EXE EXE	PRO EXE EXE EXE CLK1 CLK2 CLK3 CLK4 CLK5 CLK6 CLK7 PRO EXE EXE EXE EXE EXE PRO EXE EXE EXE EXE EXE EXE	PRO EXE EXE FRO EXE FRO EXE FRO FRO EXE FRO FRO <td> PRO EXE EXE</td>	PRO EXE EXE

Matter No.: 10559-011003 Applicant(s): Altug Koker, et al.

INTEGRATED CHIPSETS HAVING DATA REORDERING

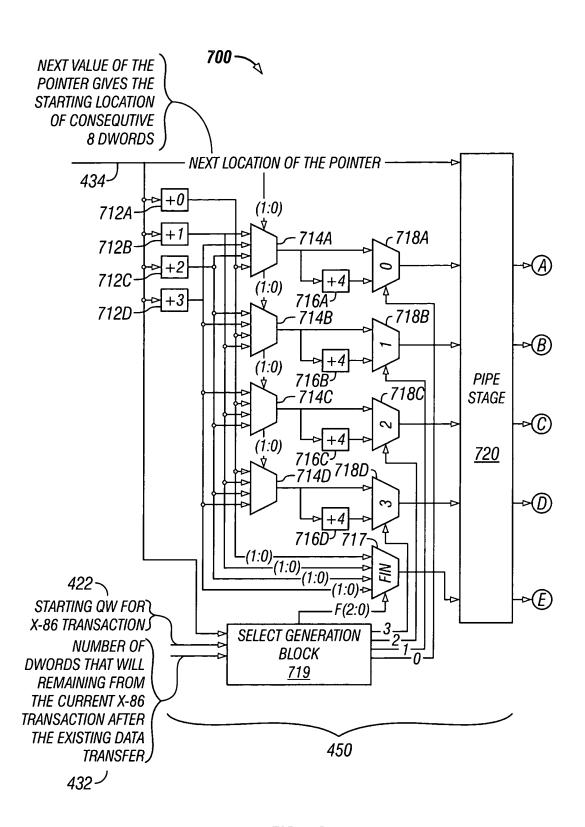


FIG. 7A

Matter No.: 10559-011003
Applicant(s): Altug Koker, et al

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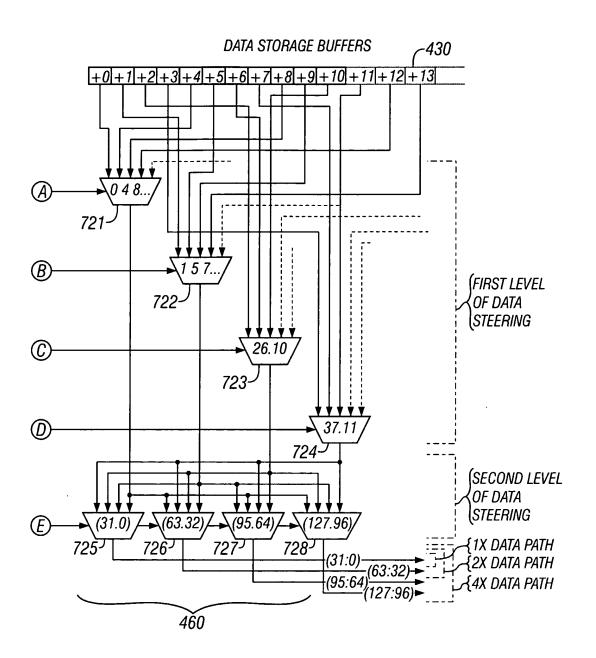
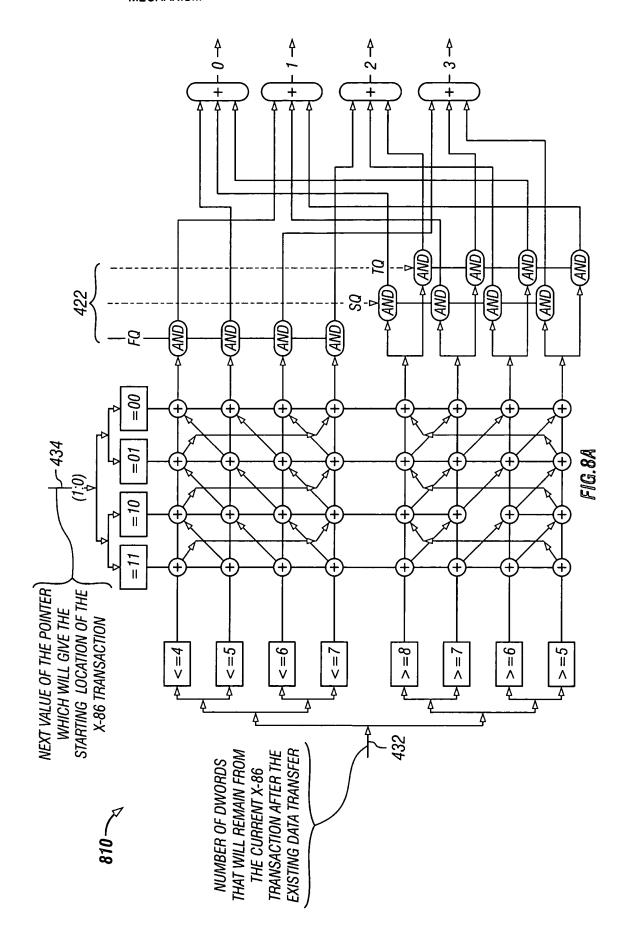


FIG. 7B

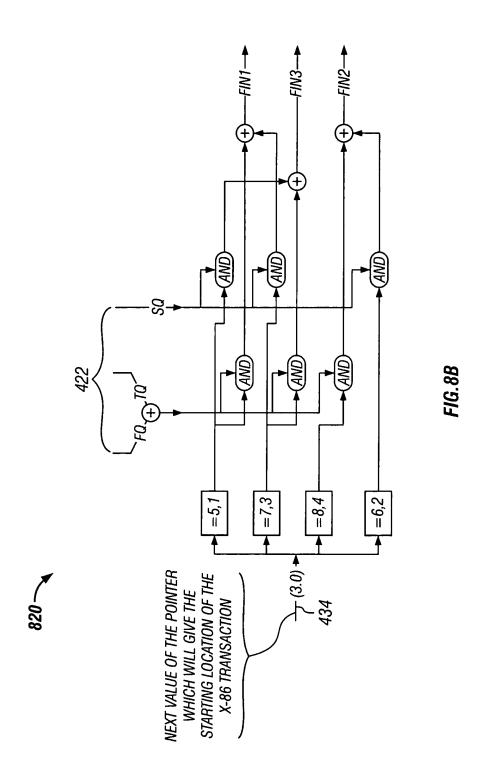
Page 9 of 12

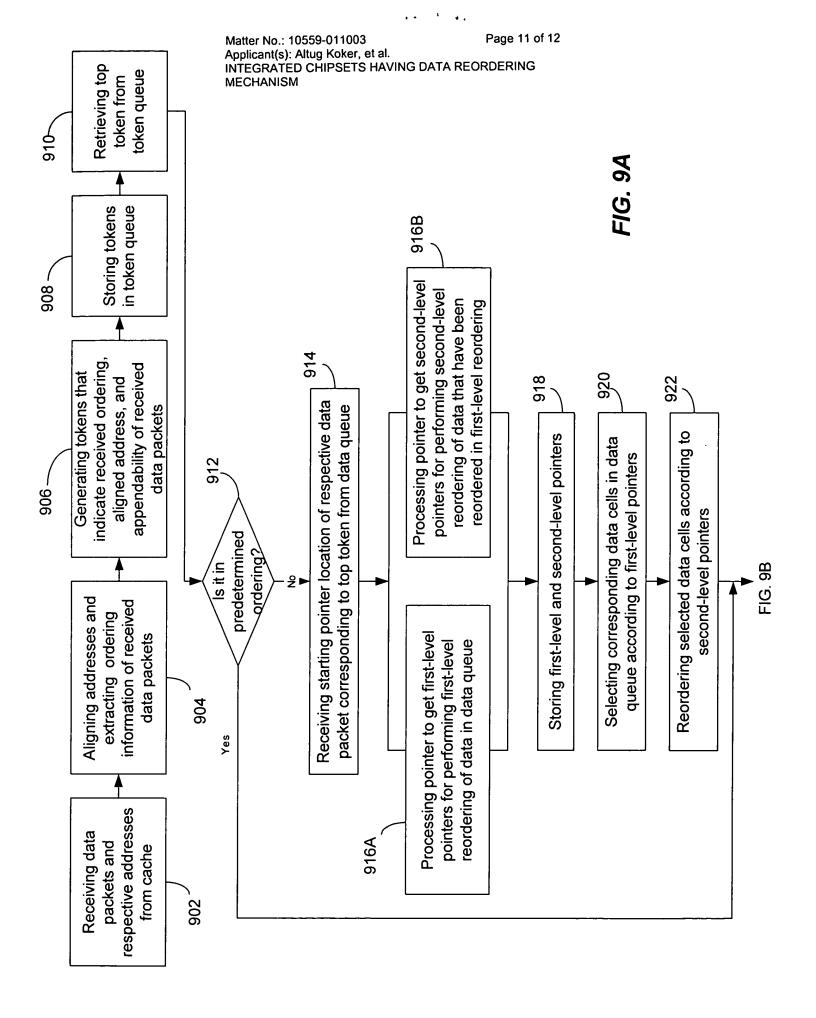
Matter No.: 10559-011003

Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING



Matter No.: 10559-011003 Page 10 of Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING MECHANISM Page 10 of 12





Page 12 of 12

Matter No.: 10559-011003 Page 12 of Applicant(s): Altug Koker, et al.
INTEGRATED CHIPSETS HAVING DATA REORDERING

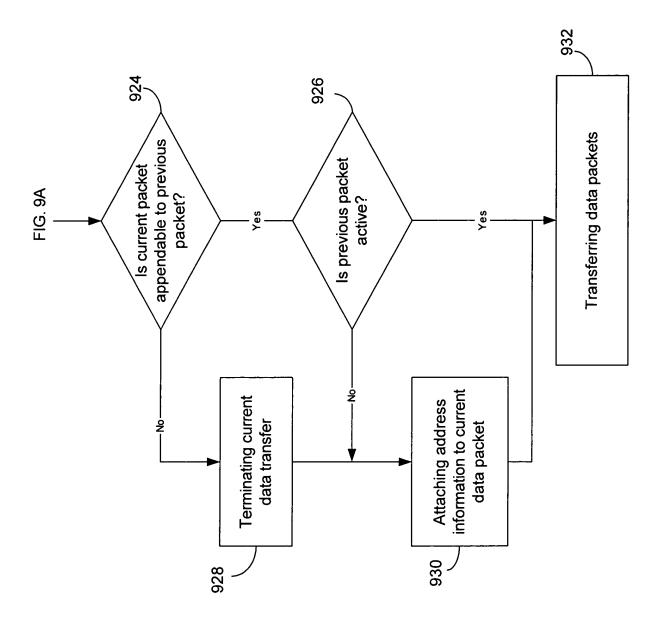


FIG. 9B